



Sheet 1 of 1

Form 1449*	Atty. Docket No.: 303.586US1	Serial No. 09/320,421
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
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## U.S. PATENT DOCUMENTS

**Examiner	Document Number	Date	Name	Class	Subclass	Filing Date
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## FOREIGN PATENT DOCUMENTS

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Initial						Yes   No

## OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner	
Initial	
BT	Denton, J.P., et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate", <u>IEEE Electron Device Letters</u> , 17(11), pp. 509-511, (November 1996)
BT	Frank, D.J., et al., "Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?", <u>IEDM</u> , pp. 553-556, (1992)
BT	Frank, J., et al., "Monte Carlo Simulations of p- and n-Channel Dual-Gate Si MOSFET's at the Limits of Scaling", <u>IEEE Transactions on Electron Devices</u> , 40(11), pg. 2103, (November 1993)
BT	Mizuno, T., et al., "High Performance Characteristics in Trench Dual-Gate MOSFET (TDMOS)", <u>IEEE Transactions on Electron Devices</u> , 38(9), pp. 2121-2127, (1991)

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Date Considered

2/11/02

\*Substitute Disclosure Statement Form (PTO-1449)

\*\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.